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Japanese Laid-open Patent

Laid-open Number:	Hei 5-267480
Laid-open Date:	October 15, 1993
Application Number:	Hei 4-94796
Filing Date:	March 21, 1992
Applicant:	Ricoh Company, Ltd.

[Title of the Invention]

SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

[Abstract] (Corrected)

[Object] Bad influence is not exerted on device characteristics by reducing the amount of carbon atoms taken into a silicon oxide film, when the silicon oxide film is formed by the plasma CVD method with organic oxysilane such as TEOS, as a main raw material.

[Construction] A silicon substrate 26 is arranged on a lower electrode 23, and is heated by a lamp 22. A reaction gas is supplied through a gas supply port 29, and a high frequency voltage is applied between both electrodes 23 and 24 from a high frequency power source 28. Thus, the reaction gas reacts, and a BPSG film or a PSG film is deposited on the silicon substrate 26. In a plasma CVD condition, the pressure within a CVD reaction chamber 21 is set to 6.5 Torr, a substrate temperature is set to range from 300 to 450°C, and power of the

high frequency power source 28 is set to range from 100 to 500 W, and the TEOS is held at 40°C. The BPSG film is deposited while helium gas is ventilated and the TEOS is supplied as the reaction gas from the gas supply port 29 to the reaction chamber 21 together with oxygen, TMP and TMB. An O_2 flow rate/TEOS flow rate ratio is set to 2.0 or more.

[Scope of Patent Claims]

[Claim 1] A semiconductor device characterized in that a silicon oxide film having a small content of carbon and deposited by the plasma CVD method with organic oxysilane as a principal component is used as an interlayer insulating film formed below metal wiring of the semiconductor device.

[Claim 2] A semiconductor device according to claim 1, wherein said interlayer insulating film is an interlayer insulating film between gate wiring and metal wiring.

[Claim 3] A method of manufacturing a semiconductor device characterized in that organic oxysilane is used as a main raw material, and a ratio of an oxygen flow rate and an organic oxysilane flow rate is set to 2.0 or more in O_2/(organic oxysilane) as a flow rate ratio when the organic oxysilane is represented in ventilating gas flow rate, in a method for depositing an interlayer insulating film of the semiconductor device by the plasma CVD method.

[Claim 4] A method of manufacturing a semiconductor device according to claim 3, wherein said interlayer insulating film is an interlayer insulating film between gate wiring and metal wiring.

[Detailed Description of the Invention]

[0001]

[Field of the Industrial Application] The present invention relates to a semiconductor device having a silicon oxide film as an interlayer insulating film, and a manufacturing method for depositing this interlayer insulating film of the silicon oxide film by the plasma CVD method.

[0002]

[Prior Art] A method using TEOS (tetra ethyl ortho silicate) as a principal component of an interlayer insulating film of a semiconductor device by the plasma CVD method is used. A silicon oxide film formed by this method is excellent in step coverage in comparison with a silicon oxide film formed by a normal pressure CVD method with silane as a main raw material. Further, film quality is stable in comparison with the silicon oxide film formed by the normal pressure CVD method with the TEOS as a main raw material.

[0003] The silicon oxide film, such as a BPSG film, a PSG film, is widely used as an interlayer insulating film between gate wiring (polysilicon or polycide, etc.) of a MOS type

semiconductor device, and a first layer metal wiring. The plasma CVD method using the TEOS as a main raw material to provide good step coverage as the interlayer insulating film and improve flatness after reflow is adopted. However, in the silicon oxide film formed by the plasma CVD method with the TEOS as a main raw material, an organic component generated in a forming process of the silicon oxide film, strongly tends to be taken into the silicon oxide film. Silane (SiH_4) as a forming material of the insulating film as a main current at present, does not include the organic component in its molecular structure. Accordingly, carbon is not included in the silicon oxide film formed with silane as a main raw material.

[0004] When the silicon oxide film formed by the plasma CVD method with the TEOS as a main raw material is utilized as the interlayer insulating film between metal wirings, a carbon atom taken into the silicon oxide film is stable, and does not have bad influence on characteristics of the semiconductor device. However, when this silicon oxide film is used in the interlayer insulating film between and gate wiring and metal wiring, heat treatment (reflow process) is normally performed for the purpose of flattening and activation of injected impurities after the CVD film is formed. Accordingly, the carbon atom taken into the silicon oxide film formed with the

TEOS as a raw material is diffused into a semiconductor substrate by this heat treatment, and has a bad influence on device characteristics.

[0005] Therefore, several methods are proposed to prevent impurities such as carbon from being taken into the silicon oxide film formed by the plasma CVD method with the TEOS as a main raw material. For example, there is a method for reducing the amount of carbon taken into the silicon oxide film by introducing the TEOS to a CVD device with nitrogen ventilation (see Japanese Patent Application Laid-Open No. Hei 1-238024). There is also a method for reducing impurities within the silicon oxide film by anneal-processing the silicon oxide film formed with the TEOS as a main raw material within an ozone atmosphere or oxygen plasma (see Japanese Patent Application Laid-Open No. Hei 3-41731). There is also a method for reducing impurities by processing the silicon oxide film by oxygen plasma or oxygen radicals so that a leak electric current is reduced (see Japanese Patent Application Laid-Open No. Hei 2-219232). There is also a method for reducing the amount of carbon taken into the oxide film by mixing hydrogen or water vapor with the TEOS (see Japanese Patent Application Laid-Open No. Hei 2-285636).

[0006]

[Problems to be solved by the Invention] An object of the

present invention is to provide a method not exerting bad influence on device characteristics by reducing the amount of carbon atoms taken into a silicon oxide film by a method different from the above proposed methods, when the silicon oxide film is formed by the plasma CVD method with organic oxysilane such as TEOS as a main raw material, and provide a semiconductor device having an interlayer insulating film formed in this way.

[0007]

[Means for solving the Problems] In a semiconductor device of the present invention, a silicon oxide film having a small content of carbon and deposited by the plasma CVD method with organic oxysilane as a principal component is used as an interlayer insulating film formed below a metal wiring. In a preferable mode, this interlayer insulating film is an interlayer insulating film between a gate wiring and a metal wiring. In a method of manufacturing the present invention, organic oxysilane is used as a main raw material, and a ratio of an oxygen flow rate and an organic oxysilane flow rate is set to 2.0 or more in O_2/(organic oxysilane) as a flow rate ratio when the organic oxysilane is represented in ventilating gas flow rate in deposition of the interlayer insulating film of the semiconductor device using the plasma CVD method.

[0008] $C_2H_5Si(OC_2H_5)_3$, $Si(OC_3H_7)_4$, $Si(OCH_3)_4$, etc. can be used as

the organic oxysilane as a main raw material in formation of the silicon oxide film by the plasma CVD method, in addition to the TEOS. When the organic oxysilane is guided to a reaction chamber, an inert gas such as helium and oxygen are ventilated to the organic oxysilane which is suitably heated, and the organic oxysilane is guided to the reaction chamber together with this ventilating gas. Further, the organic oxysilane is heated and its vapor may be also guided to the reaction chamber. At a ventilating time in the case of the TEOS, it is suitable to set the temperature of the TEOS to range from 30 to 50°C.

[0009]

[Embodiment] Fig. 1 shows one embodiment of a semiconductor device of the present invention. An active area is formed in a silicon substrate 2 by a field oxide film 4. A source area 6 and a drain area 8 are formed in this active area by impurity diffusion. A gate electrode 12 of polysilicon is formed on a channel area between the source area 6 and the drain area 8 through a gate oxide film 10. A BPSG film or a PSG film as a silicon oxide film having a small content of carbon and deposited by the plasma CVD method with the TEOS as a principal component is formed as an interlayer insulating film 14 between the gate electrode 12 and metal wirings 16 and 18. A contact hole is formed in the interlayer insulating film 14,

and the metal wirings 16 and 18 are respectively connected to the source area 16 and the drain area 8.

[0010] Fig. 2 schematically shows a plasma CVD device used in a method of manufacturing the present invention. In Fig. 2, a lower electrode 23 and an upper electrode 24 are arranged within a reaction chamber 21. Temperature of the lower electrode 23 is controlled by a lamp 22, and the lower electrode 23 is connected to the ground. The upper electrode 24 has a shower head for emitting a reaction gas and is also used as a high frequency application electrode. A vacuum exhausting operation of the reaction chamber 21 is performed through an exhaust port 25. A silicon substrate 26 for depositing the silicon oxide film thereon is arranged on the lower electrode 23, opposite to the upper electrode 24. The TEOS is ventilated by an inert gas such as helium or oxygen, and is supplied from a gas supply port 29 to the reaction chamber 21 together with helium or oxygen of this ventilating gas. Oxygen and an impurity raw material gas such as TMP (trimethyl phosphate; $PO(OCH_3)_3$, TMB (trimethyl borate; $B(OCH_3)_3$) are also supplied from the gas supply port 29 to the reaction chamber 21, in addition to the ventilating gas including the TEOS. These reaction gases are uniformly supplied from the shower head of the upper electrode 24 onto the silicon substrate 26, and are exhausted from the exhaust

port 25. A high frequency voltage of 13.56 MHz is applied by a high frequency power source 28 between the upper electrode 24 and the lower electrode 23.

[0011] The silicon substrate 26 is arranged on the lower electrode 23 in the CVD device of Fig. 2. The substrate 26 is heated through the lower electrode 23 by light incident into the reaction chamber 21 from the lamp 22 through a quartz glass 27. The reaction gases are supplied through the gas supply port 29, and the high frequency voltage is applied between both electrodes 23 and 24 from the high frequency power source 28, so that the reaction gases react and a BPSG film or a PSG film is deposited on the silicon substrate 26.

[0012] In a plasma CVD condition, the pressure within the CVD reaction chamber 21 is set to range from 2 to 12 Torr, and is set to e.g., about 6.5 Torr. The substrate temperature is set to range from 300 to 450°C, and power of the high frequency power source 28 is set to range from 100 to 500 W. The TEOS has 99.9999% in purity, and is held at about 40°C. Fig. 3(A) shows the relation of a forming speed of the BPSG film and an O_2 flow rate/TEOS flow rate ratio when the BPSG film is deposited while helium gas is ventilated and supplied from the gas supply port 29 to the reaction chamber 21 together with oxygen, TMP and TMB. In the flow rate ratio of O_2 and the TEOS, the TEOS flow rate is represented as a helium gas flow rate

when the helium gas is ventilated to the TEOS held at 40°C and the TEOS is vaporized and guided to the reaction chamber 21 together with the helium gas. In accordance with Fig. 3(A), as the O_2 flow rate/TEOS flow rate ratio is reduced, the forming speed of the BPSG film is increased. This ratio is generally set and used in a range from 0.5 to 2.0 in consideration of productivity. However, it has been found that a large amount of carbon is taken into the BPSG film formed in such a range, and has a bad influence on device characteristics. Fig. 3B shows the relation of the O_2 flow rate/TEOS flow rate ratio and the content of carbon within the BPSG film at a forming time of the BPSG film. The carbon content is measured by the SIMS (secondary ion mass spectrometry). After the BPSG film is formed, the reflow process (920°C, nitrogen atmosphere, 30 minutes) of a sample is performed. This sample is analyzed by the SIMS, and the peak concentration of carbon segregated at an interface of the BPSG film and the silicon substrate is shown. The concentration of carbon within the BPSG film with silane as a main raw material is about 50×10^{18} atoms/cc, and is approximately the same as a background value of the SIMS analysis.

[0013] The influence of carbon taken into the BPSG film on the device characteristics most notably appears in the resistance of a P-type diffusion layer of a CMOS device. As the taken-in

carbon amount is increased, the resistance of the P-type diffusion layer tends to be increased. Fig. 3C shows the relation of the O_2 flow rate/TEOS flow rate ratio and a sheet resistance value of the P-type diffusion layer. It should be understood that the sheet resistance value is reduced as the O_2 flow rate/TEOS flow rate ratio is increased.

[0014] The carbon amount within the BPSG film in the plasma CVD with the TEOS as a main raw material depends on the O_2 flow rate/TEOS flow rate ratio, and the influence on the device characteristics similarly depends on this ratio from the results of Fig. 3. Accordingly, it is necessary to set this ratio to be as high as possible to reduce the influence of carbon within the BPSG film as much as possible. This ratio is suitably set to a value equal to or greater than 20.

[0015] In the embodiment, the main raw material is set to the TEOS, but $C_2H_5Si(OC_2H_5)_3$, $Si(OC_3H_7)_4$, $Si(OCH_3)_4$ can be also used as organic oxysilane in addition to the TEOS. When these materials of organic oxysilane are set to main raw materials, carbon similarly tends to be taken into these materials. Accordingly, in these cases, the taken-in carbon amount can be also reduced by setting an O_2 flow rate/(organic oxysilane) flow rate ratio to be equal to or greater than 20 in the present invention.

[0016]

[Effect of the Invention] In the present invention, when the BPSG film and the PSG film is formed by the plasma CVD method with organic oxysilane such as TEOS as a principal component, the O_2 flow rate/(organic oxysilane) flow rate ratio is set to be equal to or greater than 2.0. Accordingly, the amount of carbon taken into a silicon oxide film such as the BPSG film, the PSG film, etc. is reduced, and an interlayer insulating film of good quality can be formed without having any bad influence on device characteristics. Since this interlayer insulating film has no bad influence on the device characteristics, this interlayer insulating film can be utilized as an interlayer insulating film between a gate wiring and a metal wiring.

[Brief explanation of the Drawings]

[Fig. 1] Fig. 1 is a cross-sectional view showing a semiconductor device of one embodiment.

[Fig. 2] Fig. 2 is a cross-sectional view schematically showing one example of a plasma CVD device to which the present invention is applied.

[Fig. 3] Fig. 3 is a view respectively showing the relation of an O_2 flow rate/TEOS flow rate ratio and a film forming speed, a carbon concentration, and a sheet resistance value in one embodiment.

[Explanation of reference numerals]

2 silicon substrate

6 source

8 drain

10 gate oxide film

12 gate electrode

14 interlayer insulating film

16, 18 metal wiring

21 reaction chamber of CVD device

22 lamp for temperature control

23 lower electrode

24 upper electrode

26 silicon substrate

28 high frequency power source

DRAWINGS

ABSTRACT

a --- EXHAUST

FIG. 2

a --- EXHAUST

FIG. 3(A)

a --- FILM FORMING SPEED (A/MINUTE)

b --- O_2/TEOS RATIO

FIG. 3(B)

a --- CARBON PEAK CONCENTRATION WITHIN FILM (ATOM/cc)

FIG. 3(C)

a --- SHEET RESISTANCE (Ω/)